SoC IC

SYSTEM BUS 10

Ethernet 12

ARM 8
DI 20

DSP 6
DI 18

GPP 4
DI 16

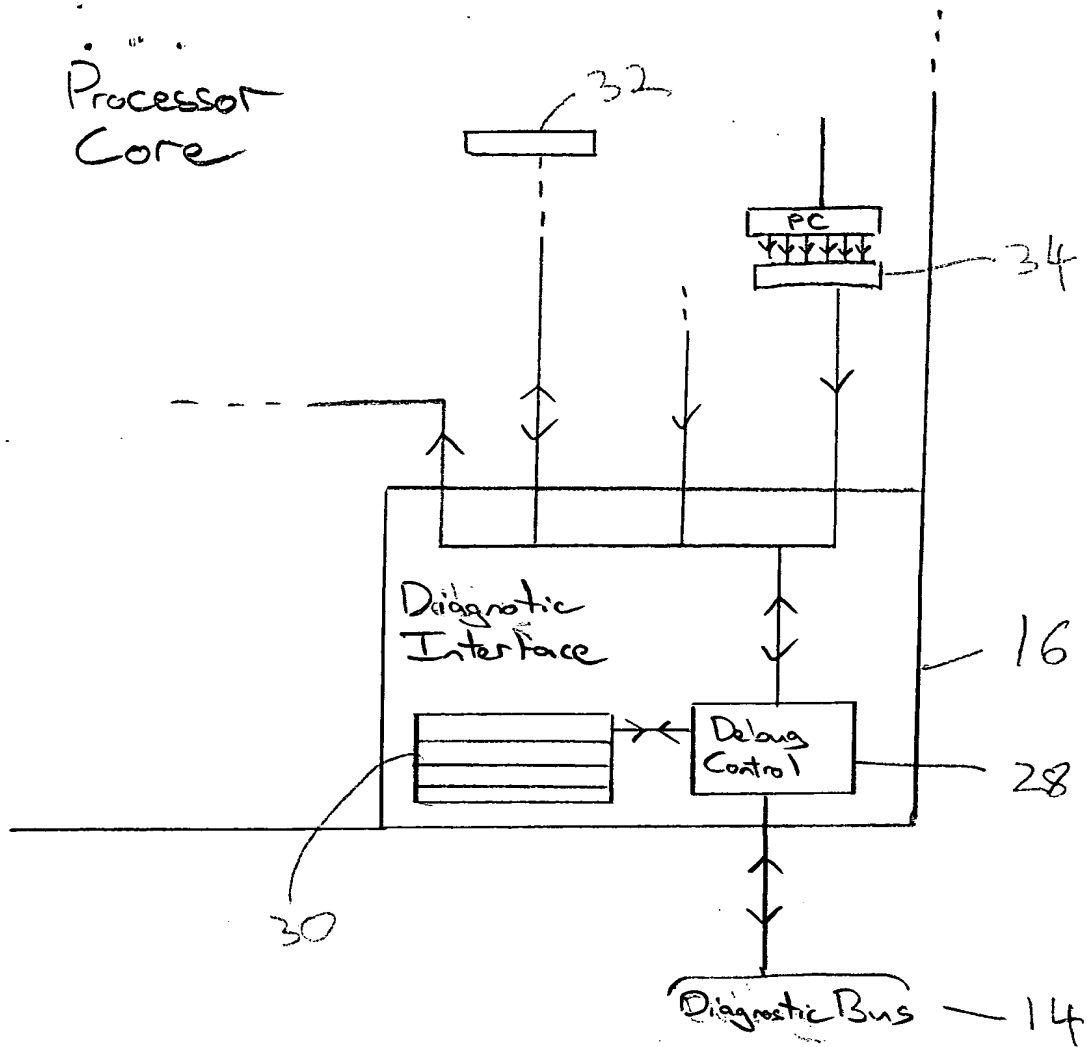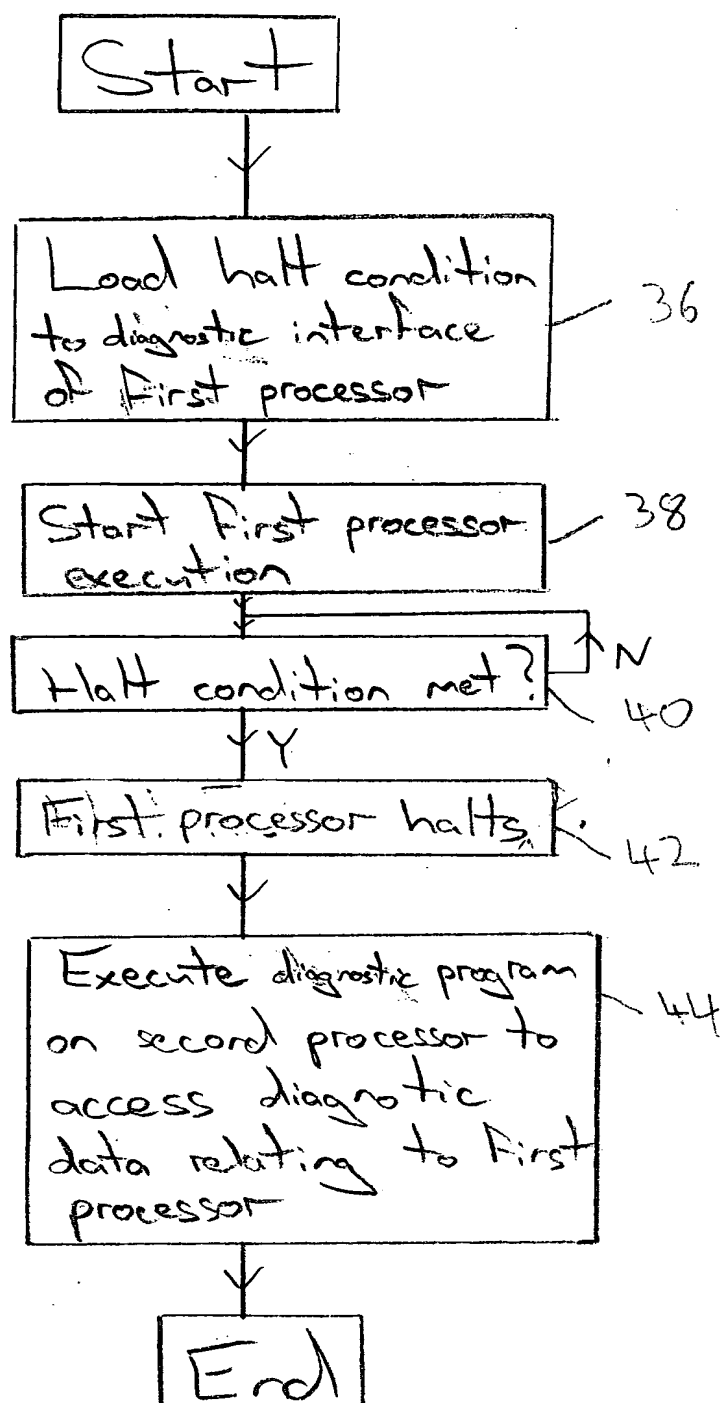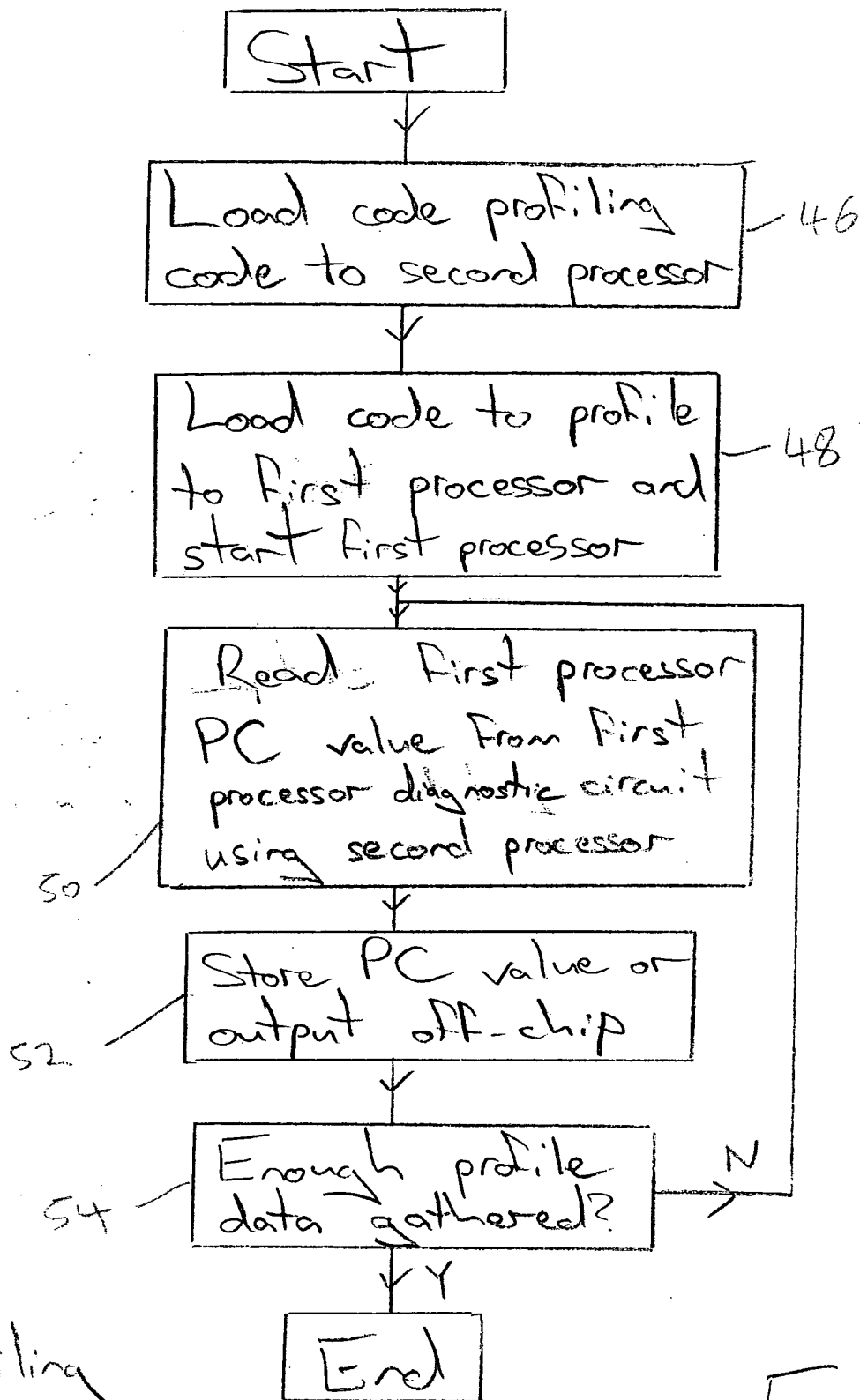Debug Access Port + Bridge 22

DIAGNOSTIC BUS 14

Protocol Translator 23

24

26

Fig. 1

BEST AVAILABLE COPY

Processor
Core

32

PC

34

Diagnostic
Interface

16

Debug
Control

28

30

Diagnostic Bus — 14

Fig. 2

```
                    ┌──────────┐
                    │  Start   │
                    └──────────┘
                          │
                          ▼
        ┌────────────────────────────────┐
        │ Load halt condition            │      36
        │ to diagnostic interface        │
        │ of First processor             │
        └────────────────────────────────┘
                          │
                          ▼
        ┌────────────────────────────────┐
        │ Start First processor          │      38
        │ execution                       │
        └────────────────────────────────┘
                          │
                          ▼                    ▲ N
        ┌────────────────────────────────┐───┘
        │ Halt condition met?            │      40
        └────────────────────────────────┘
                          │ Y
                          ▼
        ┌────────────────────────────────┐
        │ First processor halts,         │      42
        └────────────────────────────────┘
                          │
                          ▼
        ┌────────────────────────────────┐
        │ Execute diagnostic program     │      44
        │ on second processor to         │
        │ access diagnostic              │
        │ data relating to First         │
        │ processor                       │
        └────────────────────────────────┘
                          │
                          ▼
                    ┌──────────┐
                    │   End    │
                    └──────────┘
```

Halting Mode
Diagnosis

Fig. 3

Start

Load code profiling
code to second processor ——46

Load code to profile
to first processor and
start first processor ——48

Read: First processor
PC value from first
processor diagnostic circuit
using second processor
50

Store PC value or
output off-chip
52

Enough profile
data gathered? ——54   N

Y

End

Code Profiling
Debug

Fig. 4